Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **INPUT –**
2. **INPUT +**
3. **V –**
4. **OUTPUT**
5. **V +**
6. **NC**

**.034”**

**3 2**

**1**

**5 6**

**4**

**LMH6714**

**MASK**

**REF**

**.026”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref: LMH6714**

**APPROVED BY: DK DIE SIZE .026” X .034” DATE: 2/17/21**

**MFG: TEXAS INTST / NATIONAL THICKNESS .010” P/N: LMH6714**

**DG 10.1.2**

#### Rev B, 7/19/02